In the Claims:

Claim 8 (amended). The circuit configuration according to claim 6, including an inverter chain (38), said detector (33) having one of:

an XOR gate (40) with XOR inputs, one of said XOR inputs receiving an edge signal (37), and another of said XOR inputs receiving the edge signal (39) delayed through said inverter chain (38); and

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an XNOR gate with XNOR inputs, one of said XNOR inputs receiving the edge signal (37) and another of said XNOR inputs receiving the edge signal (39) delayed through said inverter chain (38).